Design and Performance Comparison of Symmetric and Asymmetric Underlap Dual-K Spacer Finfets

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Abstract: This paper investigates the innovation features of Symmetric and Asymmetric FinFET devices with dual-k spacer over traditional FinFET. The designed FinFET integrates three advanced technologies i.e. FinFET, ultra-thin body (UTB) and asymmetric Dual-k spacer on a substrate of silicon-on-insulator (SOI). Recently, Dual-k dielectric spacer materials are much significant for research because of their better electrical control and provide more immunity against short channel effects (SCEs) in nanoscale devices. This work presents symmetric and asymmetric dual-k dielectric spacer in the underlap areas of FinFET and performance has been analyzed.

Keywords: FinFETs, Dual –k Spacers, Short Channel Effects, Underlap devices.

Introduction

To keep pace with Moore's law, consecutive scaling in MOSFET technology allows the higher chip density and more area utilization. With downscaling, certain short channel effects come into play which adversely affects the device performance. New structures like double gate MOSFET, symmetric or asymmetric MOSFET, MOSFETs with metal gate and high-k dielectrics were designed. One of the highly appreciable designs in the semiconductor history is 3-D FinFET technology that has highly facilitated the progress of electronics industry. Leading manufacturing companies like Intel and TSMC have adopted FinFET in their 22-nm and 16-nm technology nodes while others will be using in the near future (Pal et al. 2013). This improvement in technology permits long battery lifetime and can be applied in low power (LP) and high performance (HP) applications.

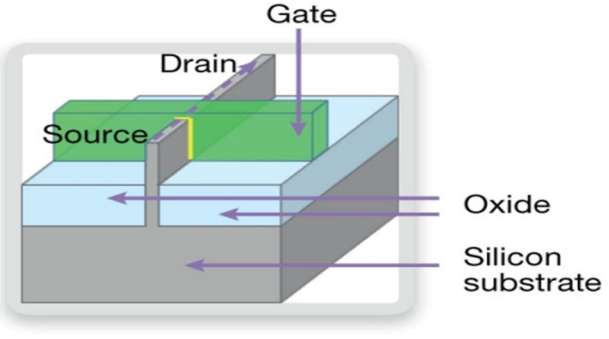


Figure 1. FinFET (Swinnen and Duncan. 2013)

Comparison of Symmetric and Asymmetric underlap Dual – k Spacer FinFETs with different Spacers like HfO_2 and $Si3N_4$ have been designed at 14 nm gate length using TCAD and then performance of all these FinFETs is calculated in terms of voltage-current Characteristics and SCEs like Drain Induced Barrier Lowering (DIBL) and Subthreshold Swing (SS). Then the Impact of Dual – k Spacer on the FinFETs device performance is analyzed. Further improvement in FinFET devices has been carried out such as underlap FinFETs (Sachid et al. 2008; Koley et al. 2013), spacer based technology (Pal et al. 2014), and finally dual-k Spacer FinFETs .The dual-k spacer FinFETs combines various technologies such as (i) ultra-thin-body (UTB), (ii) 3-D FinFET, and (iii) spacer engineering in silicon-on-insulator (SOI) substrate.

Device design and process parameters

Device Design Procedure

For designing the FinFET with different spacers various process parameters have been used which are listed in Table 1. Trigate(TG) FinFET has been designed where gate covers the fin from three sides. Gate material is used of titanium (Ti) metal. Ultra-thin body is of SiC3C material. Two different k spacers have been used; one is $Si3N_4$ (k=7) and HfO_2 (k=21) is second dielectric which has been used to allow further scaling of gate oxide.

Table 1. Design Parameters for simulation

Parameters	Nomenclature	Conventional FinFET
W_{Fin}	Fin Width	10nm
H_{Fin}	Fin height	16nm
L_g	Gate length	14nm
L_{sp}	Spacer Length	5nm
UTB	Ultra thin body thickness	6.5nm
EOT	Gate oxide thickness	0.9nm
L_T	Total device length	95nm
W_T	Total device width	32.2nm
BOX	Buried oxide thickness	40nm
$\Phi_{\varphi m}$	Work function of gate metal	4.3eV

Size of Mesh Constraint in Substrate Region: 0.04 µm, Active Region: 0.050 µm,Transistor Channel: 0.001µm

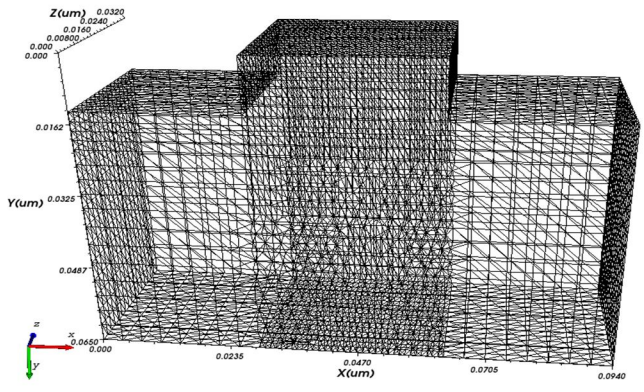


Figure 2. Mesh of Whole FinFET

Symmetric and Asymmetric Spacer FinFET architecture

Symmetric Low – k Spacer FinFET

Symmetric Low – k Spacer was designed with parameters: L_g=14 nm; T_{ox} = 0.9 nm; channel doping $N_A=1\times10^{18}$ cm^{-3}; source /drain doping $N_D= 10^{20}$ cm^{-3}; H_{fin} =16nm and W_{fin} =10nm of the designed Low – k Spacer FinFET as shown in Figure 3.

Symmetric High – k Spacer FinFET

Symmetric High – k Spacer was designed with parameters: L_g=14nm; T_{ox}= 0.9 nm; channel doping $N_A=1\times10^{21}$ cm^{-3}; source /drain doping $N_D= 10^{20}$ cm^{-3}; H_{fin}=16nm and W_{fin}= 10 nm of the designed High – k Spacer FinFET is shown in Figure 4.

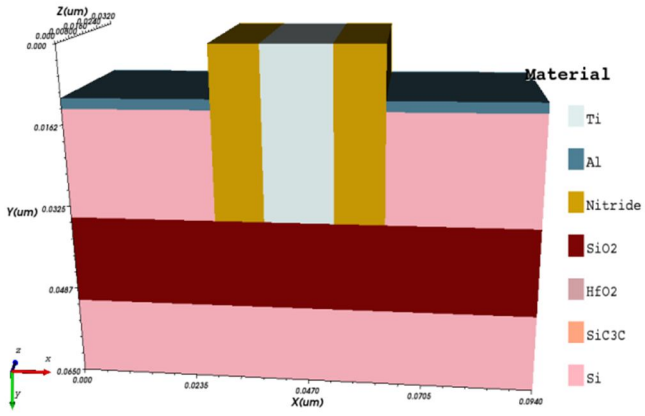


Figure 3.Symmetric Low-K Spacer FinFET

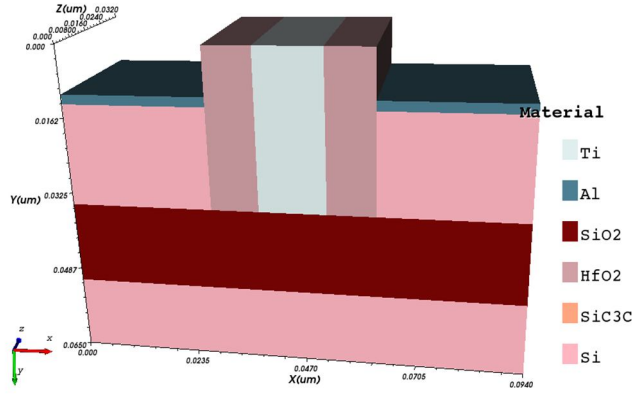


Figure 4.Symmetric High-K Spacer FinFET

Asymmetric Spacer FinFET

Asymmetric Spacer was designed with parameters: L_g =14 nm; T_{ox} = 0.9 nm; channel doping $N_A = 9\times10^{21}$ cm^{-3}; source /drain doping $N_D = 10^{18}$ cm^{-3}; H_{fin} =16n and W_{fin}= 10 nm of the designed Asymmetric Spacer FinFET is shown in Figure 5.

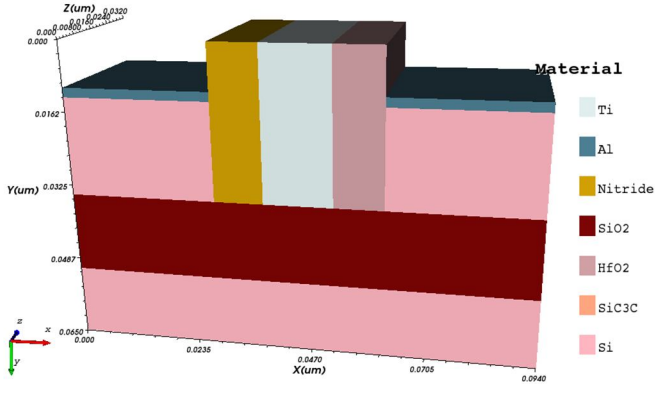


Figure 5. Asymmetric Spacer FinFET

Asymmetric Dual – k Spacer FinFET

Asymmetric Dual-k Spacer was designed with parameters: L_g =14 nm; T_{ox} = 0.9 nm; channel doping $N_A = 9\times10^{21}$ cm^{-3}; source /drain doping $N_D = 10^{18}$ cm^{-3}; H_{fin} =16nm and W_{fin}= 10 nm of the designed Asymmetric dual-k Spacer FinFET is shown in Figure 6.

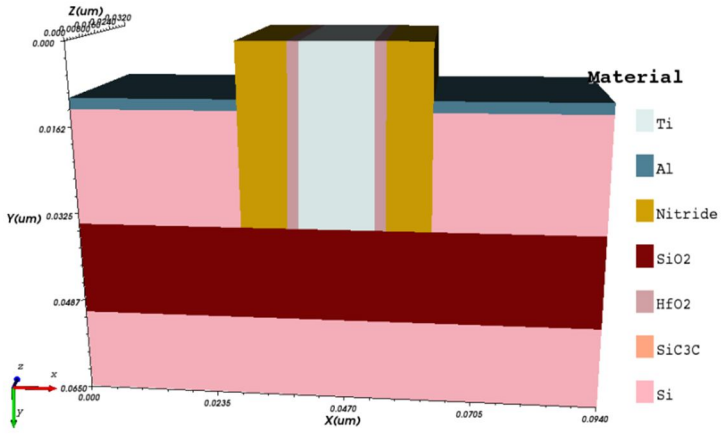


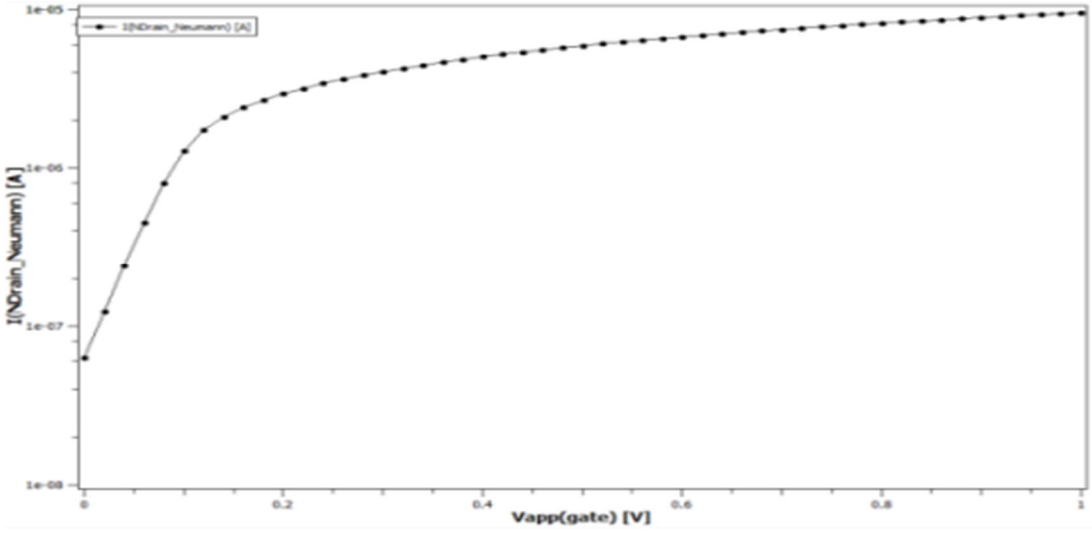
Figure 6.Asymmtric Dual –k Spacer FinFET

Results and discussion

The performance of the designed symmetric and asymmetric underlap dual - k Spacer FinFETs with different Spacers at 14 nm gate length have been analyzed in terms of Voltage-Current density gradient model has been used instead of classical different diffusion model because quantum mechanical effects are much severe for less than 20nm gate length. Analytic mobility model has been used.

Analysis of FinFETs

Performance of all designed FinFETs has been analyzed through 3D TCAD numerical devices simulations. The on-current (I_{ON}) and off-current (I_{OFF}) have been calculated at gate voltage Vg = 1 and 0 V respectively. Subthreshold Swing (SS) is defined as dVg / dlog(Id) measured from transfer characteristics. The Drain-induced barrier lowering (DIBL) is measured from transfer characteristics of all FinFETs. The transfer characteristics have been shown in linear as well logarithmic scale for drain voltage of 0.05 V. Drain-induced barrier lowering has been calculated corresponding to V_{ds}=0.02 V and 1 V.
$W_{eff} = 2H_{fin} + W_{fin}$.
DIBL has been evaluated at this current $I = W_{eff}*10^{-7}$ i.e. 3×10^{-7} A.
Transfer characteristics of Low-k Spacer FinFETs, High-k Spacer FinFETs, Asymmetric Spacer FinFETs, Asymmetric Dual-k Spacer FinFETs have been obtained for Vds=0.02V, 0.05V and 1 V. which have been shown in figure 7 to figure 10.



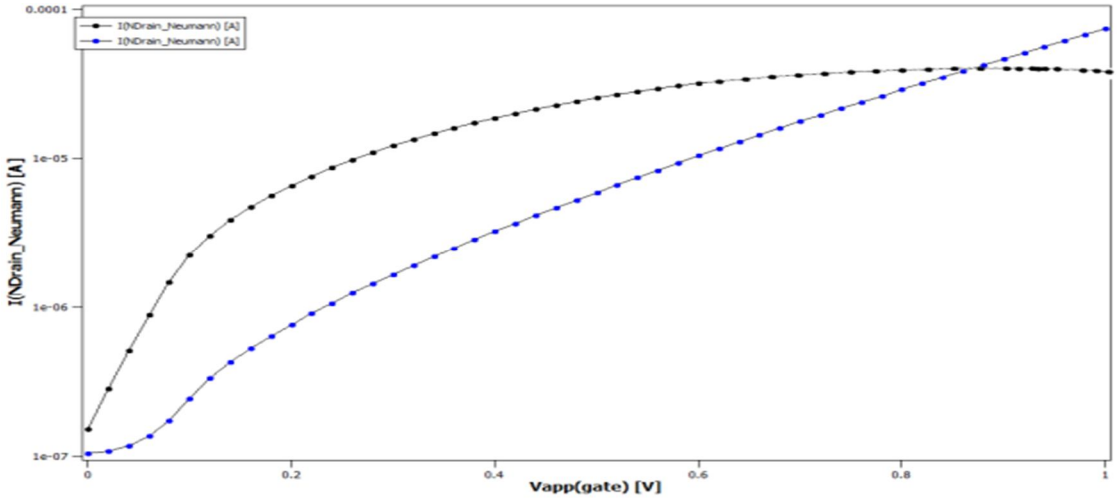


Figure 7.**a)** Low – k Spacer FinFETat Vds=0.05V, **b)** Low – k Spacer FinFET at Vds=0.02 V and 1V

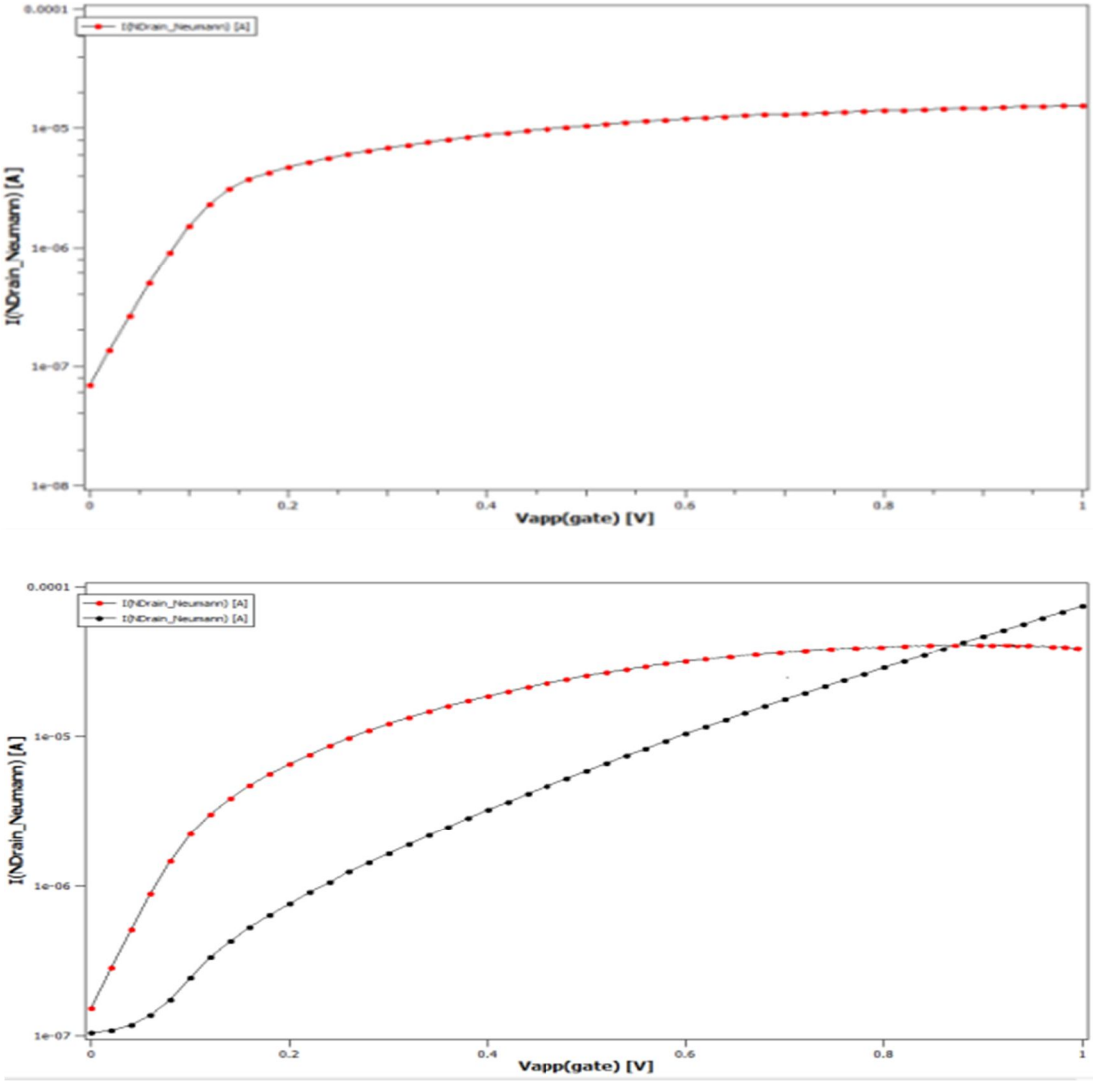
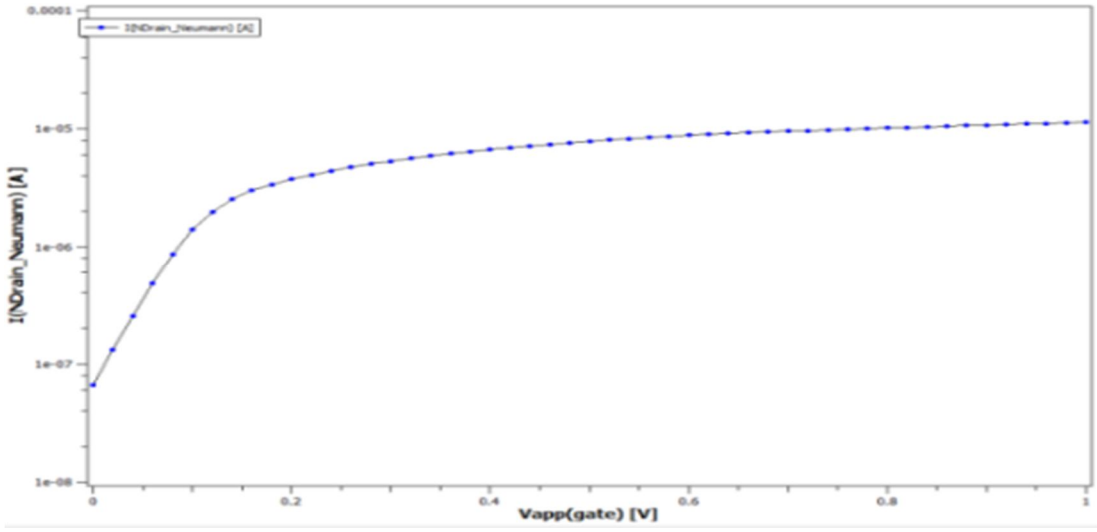


Figure 8. **a)** High – k Spacer FinFET at Vds=0.05V, **b)** High – k Spacer FinFET at Vds=0.02 V and 1V



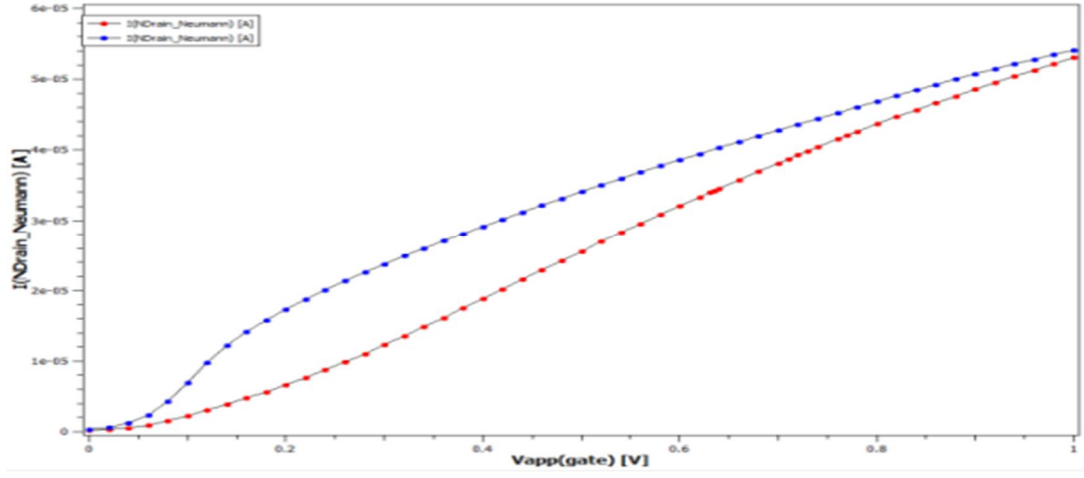
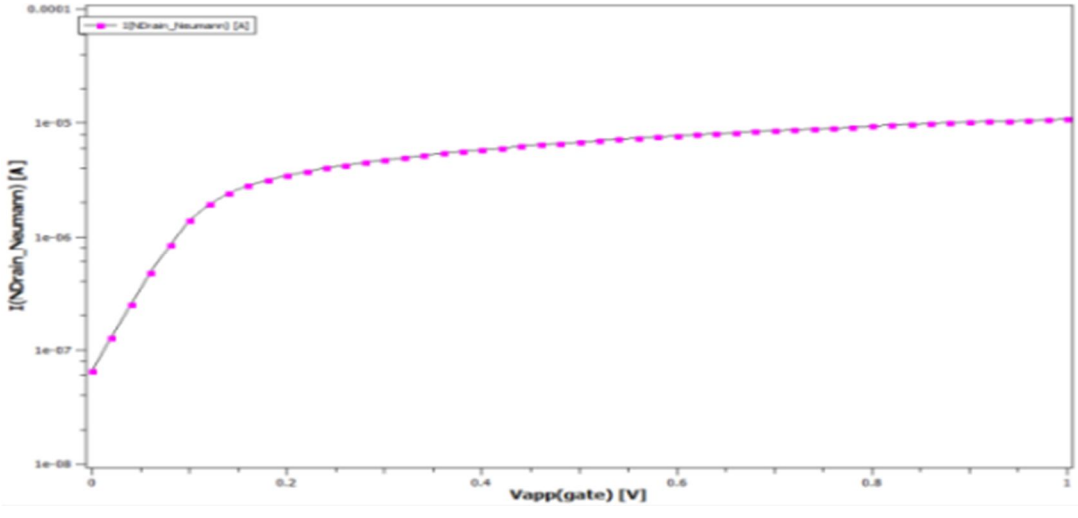


Figure 9.**a)** Asymmetric Spacer FinFET at Vds=0.05V, **b)** Asymmetric Spacer FinFET at Vds=0.02 V and 1V



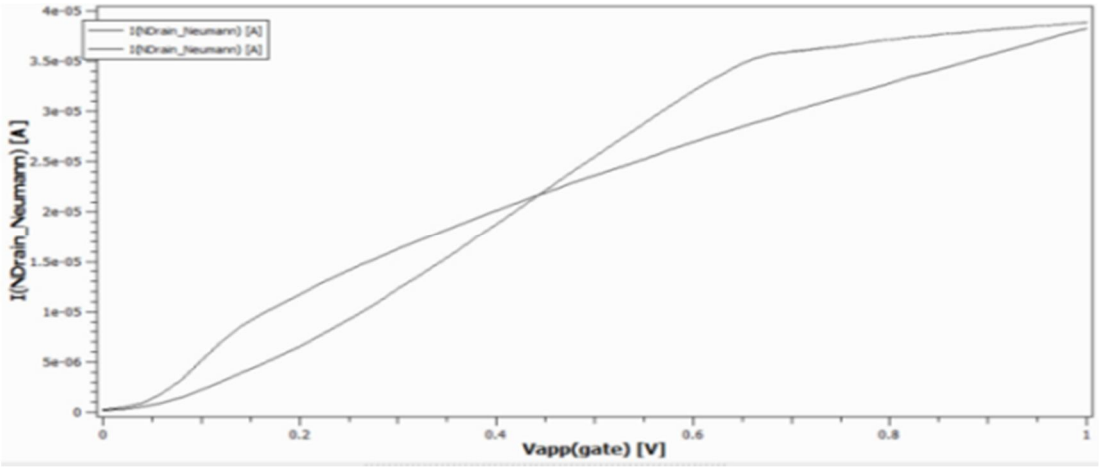


Figure 10.**a)** Asymmetric dual – k Spacer FinFET at Vds=0.05V, **b)** Asymmetric dual – k Spacer FinFET at Vds=0.02 V and 1V

Table 2.Simulation results of Low-k Spacer FinFET

Parameter	Rectangular
IOFF(A)	6.286e-08
ION(A)	9.569e-05
Subthreshold Swing (mV/dec)	61
DIBL(mV/V)	24
ION / IOFF	1.522e+03

Table 3. Simulation results of High -k Spacer FinFET

Parameter	Rectangular
IOFF(A)	6.906e-08
ION(A)	1.565e-05
Subthreshold Swing (mV/dec)	71
DIBL(mV/V)	22
ION / IOFF	2.266e+02

Table 4. Simulation results of Asymmetric Spacer FinFET

Parameter	Rectangular
IOFF(A)	6.683e-08
ION(A)	1.128e-05
Subthreshold Swing (mV/dec)	69
DIBL(mV/V)	21
ION / IOFF	1.687e+02

Table 5. Simulation results of Asymmetric Dual-k Spacer FinFET

Parameter	Rectangular
IOFF(A)	6.481e-08
ION(A)	1.082e-05
Subthreshold Swing (mV/dec)	63
DIBL(mV/V)	23
ION / IOFF	1.669e+02

On current for all the design devices has been shown in figure 11.

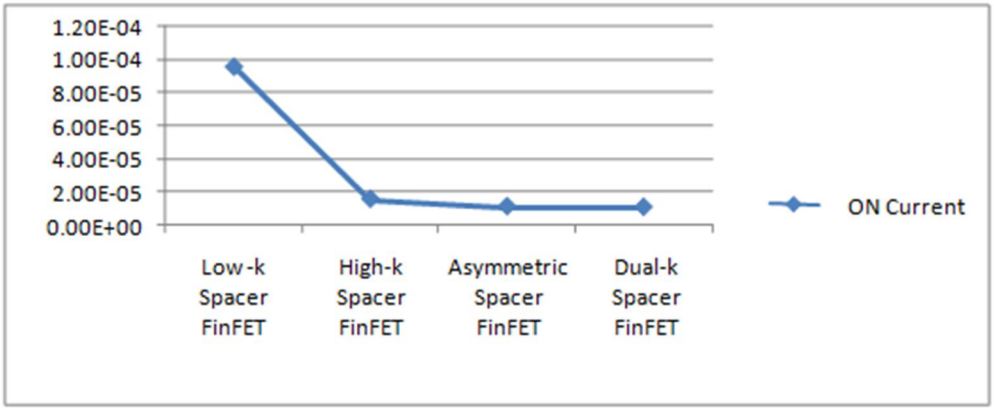


Figure 11. On Current of design devices

On current for all the design devices has been shown in figure 12.

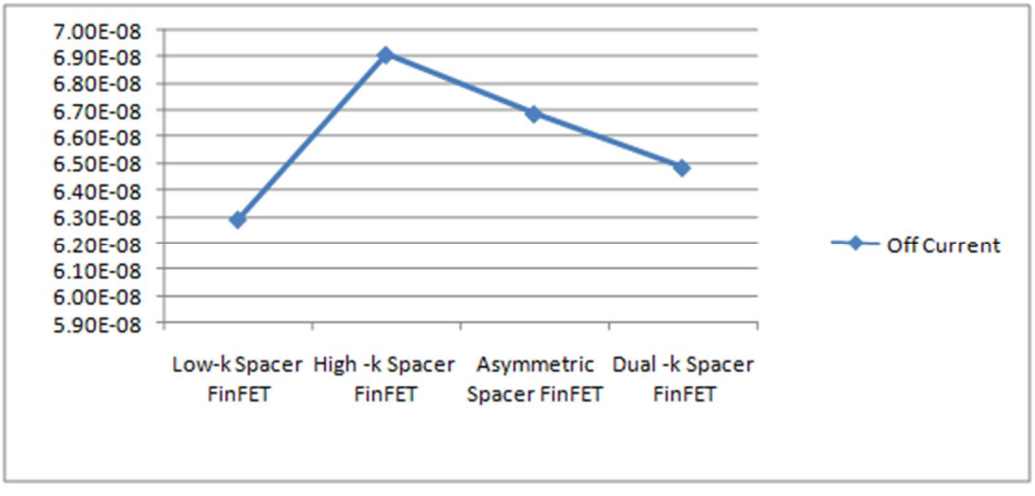


Figure 12. Off Current of design devices

Subthreshold Swing for all the design devices has been shown in figure 13.

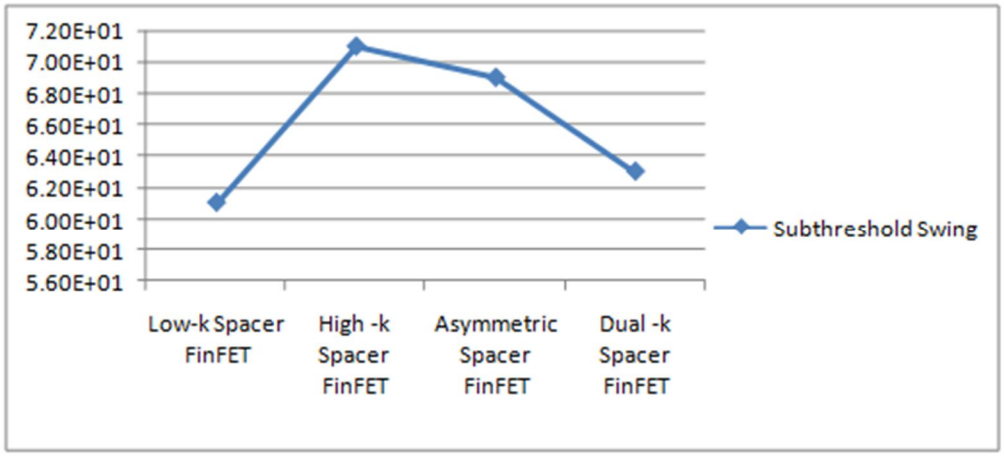


Figure 13. Subthreshold Swing of design devices

Drain Induced Barrier Lowering for all the design devices has been shown in figure 14.

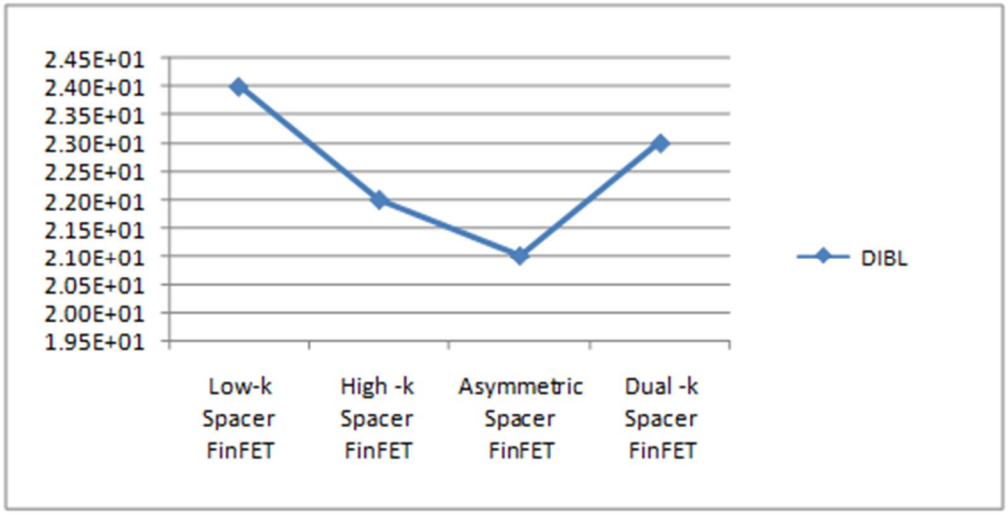


Figure 13. DIBL of design devices

Conclusion

In this work, Trigate FinFET has been designed taking low-k spacer on both sides, high-k spacer on both sides, dual-k on both sides, low-k on one side and high-k on other side for 14nm gate length. Designed devices were simulated on TCAD using density gradient model. It has been observed that dual-k spacer provides optimum SS that is close to 60mV/dec, DIBL close to 20 mV/V and off current of 6.48e-08. These devices can further be used in low leakage and low power applications.

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